DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8163TB

SILICON MMIC 2.0 GHz FREQUENCY UP-CONVERTER FOR CELLULAR TELEPHONE

DESCRIPTION

The μPC8163TB is a silicon monolithic integrated circuit designed as frequency up-converter for cellular telephone transmitter stage. The μPC8163TB has improved intermodulation performance and smaller package.

The μPC8163TB is manufactured using NEC's 20 GHz f_T NESAT™lll silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

FEATURES

- Recommended operating frequency : f_{RFout} = 0.8 GHz to 2.0 GHz, f_{IFin} = 50 MHz to 300 MHz
- Supply voltage : V_{CC} = 2.7 to 3.3 V
- High-density surface mounting : 6-pin super minimold package
- Higher IP_3 : OIP_3 = +9.5 dBm @ f_{RFout} = 830 MHz
- Minimized carrier leakage : Due to double balanced mixer

APPLICATIONS

- Digital cellular phones

ORDERING INFORMATION

Part Number	Package	Supplying Form
μPC8163TB-E3	6-pin super minimold	Embossed tape 8 mm wide. Pin 1, 2, 3 face to tape perforation side. Qty 3 kp/reel

Remark To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: μPC8163TB)

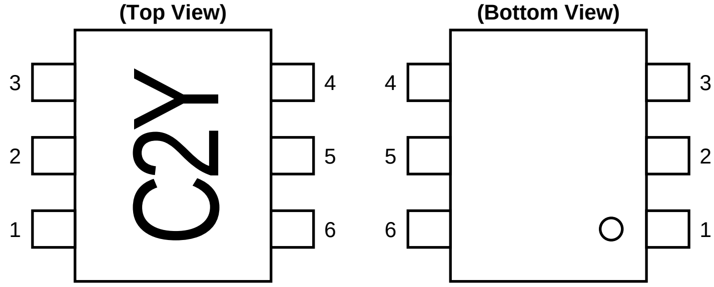
Caution Electro-static sensitive device

Document No. P13636EJ2V0DS00 (2nd edition)
Date Published June 1999 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

PIN CONNECTIONS

(Top View) (Bottom View)



Pin No.	Pin Name
1	IFinput
2	GND
3	LOinput
4	GND
5	V_{CC}
6	RFoutput

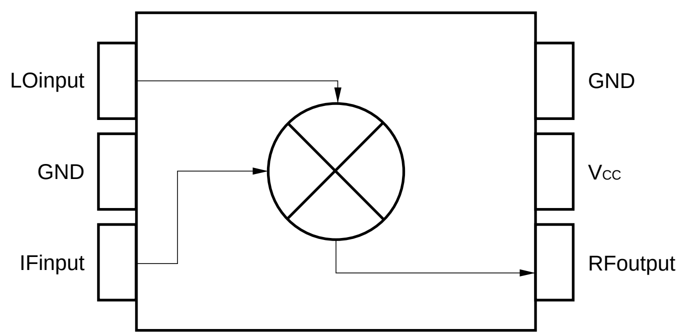
SERIES PRODUCTS (T_A = +25°C, V_{CC} = V_{RFout} = 3.0 V, Z_L = Z_S = 50 Ω)

Type	Part No.	V_{CC} (V)	I_{CC} (mA)	CG1 (dB)	CG2 (dB)	$P_{O(sat)}$ 1 (dBm)	$P_{O(sat)}$ 2 (dBm)	$OIP_3$1 (dBm)	$OIP_3$2 (dBm)
High IP_3	μPC8106TB	2.7 to 5.5	9	9	7	–2	–4	+5.5	+2.0
Low Power Consumption	μPC8109TB	2.7 to 5.5	5	6	4	–5.5	–7.5	+1.5	–1.0
Higher IP_3	μPC8163TB	2.7 to 3.3	16.5	9	5.5	0.5	–2	+9.5	+6.0

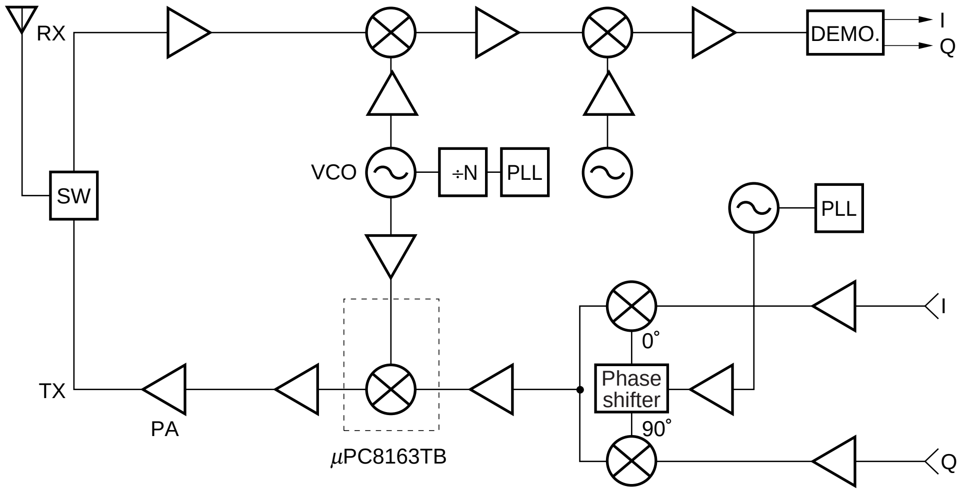
Caution The above table lists the typical performance of each model. See ELECTRICAL CHARACTERISTICS for the test conditions.

BLOCK DIAGRAM (FOR THE μPC8163TB)

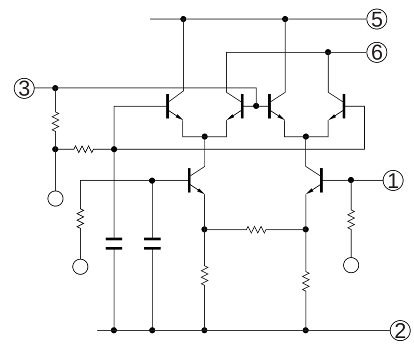
(Top View)



SYSTEM APPLICATION EXAMPLES (SCHEMATICS OF IC LOCATION IN THE SYSTEM)



PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage V	Pin Voltage V[Note]	Function and Explanation	Equivalent Circuit
1	IFinput	—	1.2	This pin is IF input to double balanced mixer (DBM). The input is designed as high impedance. The circuit contributes to suppress spurious signal. Also this symmetrical circuit can keep specified performance insensitive to process-condition distribution. For above reason, double balanced mixer is adopted.	
2 4	GND	0	—	GND pin. Ground pattern on the board should be formed as wide as possible. Track Length should be kept as short as possible to minimize ground impedance.	
3	LOinput	—	2.1	Local input pin. Recommendable input level is –10 to 0 dBm.	
5	V_{CC}	2.7 to 3.3	—	Supply voltage pin.	
6	RFoutput	Same bias as V_{CC} through external inductor	—	This pin is RF output from DBM. This pin is designed as open collector. Due to the high impedance output, this pin should be externally equipped with LC matching circuit to next stage.	

Note Each pin voltage is measured with $V_{CC} = V_{RFout} = 3.0$ V.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Rating	Unit
Supply Voltage	V_{CC}	T_A = +25°C, Pin 5 and 6	3.6	V
Power Dissipation of Package	P_D	Mounted on double-sided copperclad 50 × 50 × 1.6 mm epoxy glass PWB T_A = +85°C	200	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C
Maximum Input Power	P_{in}		+10	dBm

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	The same voltage should be applied to pin 5 and 6	2.7	3.0	3.3	V
Operating Ambient Temperature	T_A		–40	+25	+85	°C
Local Input Level	P_{LOin}	Zs = 50 Ω (without matching)	–10	–5	0	dBm
RF Output Frequency	f_{RFout}	With external matching circuit	0.8	–	2.0	GHz
IF Input Frequency	f_{IFin}		50	–	300	MHz

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{CC} = V_{RFout} = 3.0 V, f_{IFin} = 150 MHz, P_{LOin} = –5 dBm)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No Signal	11.5	16.5	23	mA
Conversion Gain 1	CG1	f_{RFout} = 830 MHz, P_{IFin} = –20 dBm	6	9	12	dB
Conversion Gain 2	CG2	f_{RFout} = 1.9 GHz, P_{IFin} = –20 dBm	2.5	5.5	8.5	dB
Maximum RF Output Power 1	$P_{O(sat)}$ 1	f_{RFout} = 830 MHz, P_{IFin} = 0 dBm	–1.5	0.5	–	dBm
Maximum RF Output Power 2	$P_{O(sat)}$ 2	f_{RFout} = 1.9 GHz, P_{IFin} = 0 dBm	–4.5	–2	–	dBm

OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY

(T_A = +25°C, V_{CC} = V_{RFout} = 3.0 V, P_{LOin} = –5 dBm)

Parameter	Symbol	Conditions		Data	Unit
Input Third Order Distortion Intercept Point	IIP_3 1	$f_{IFin}1$ = 150.0 MHz $f_{IFin}2$ = 150.4 MHz	f_{RFout} = 830 MHz	0.5	dBm
	IIP_3 2		f_{RFout} = 1.9 GHz	0.5	
Output Third-Order Distortion Intercept Point	OIP_3 1	$f_{IFin}1$ = 150.0 MHz $f_{IFin}2$ = 150.4 MHz	f_{RFout} = 830 MHz	+9.5	dBm
	OIP_3 2		f_{RFout} = 1.9 GHz	+6.0	
SSB Noise Figure	SSB NF	f_{RFout} = 830 MHz, f_{IFin} = 150 MHz		12.5	dB

TEST CIRCUIT 1 (f_{RFout} = 830 MHz)

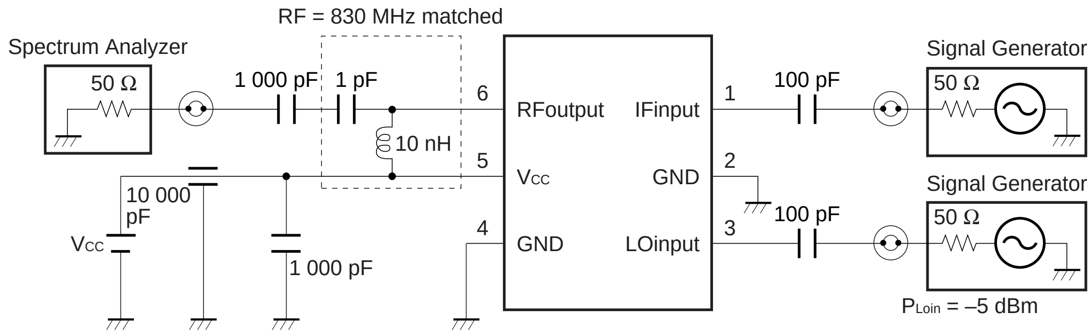
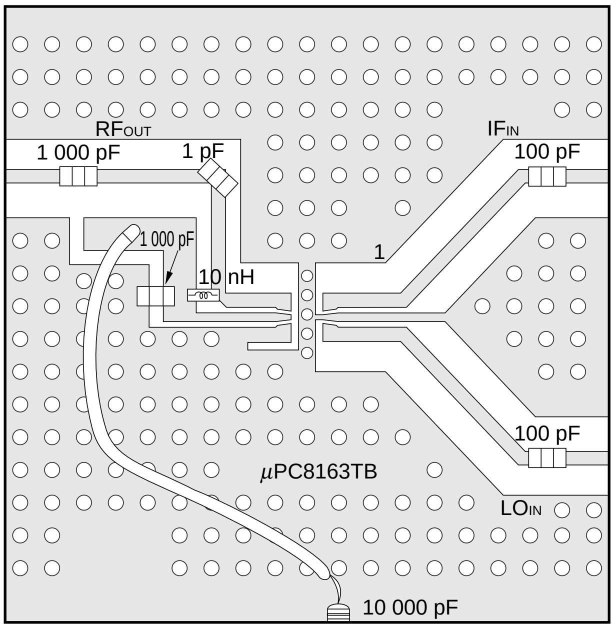


ILLUSTRATION OF TEST CIRCUIT 1 ASSEMBLED ON EVALUATION BOARD



EVALUATION BOARD CHARACTERS

(1) 35 μm thick double-sided copper clad 35 × 42 × 0.4 mm polyimide board

(2) Back side: GND pattern

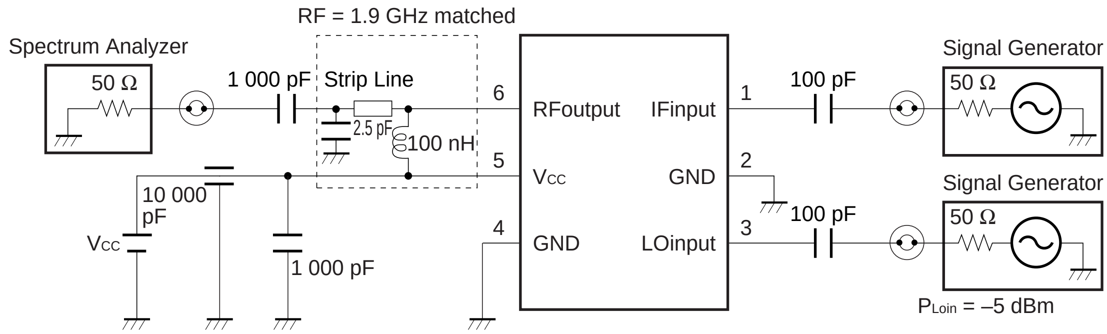
(3) Solder plated patterns

(4) ○O: Through holes

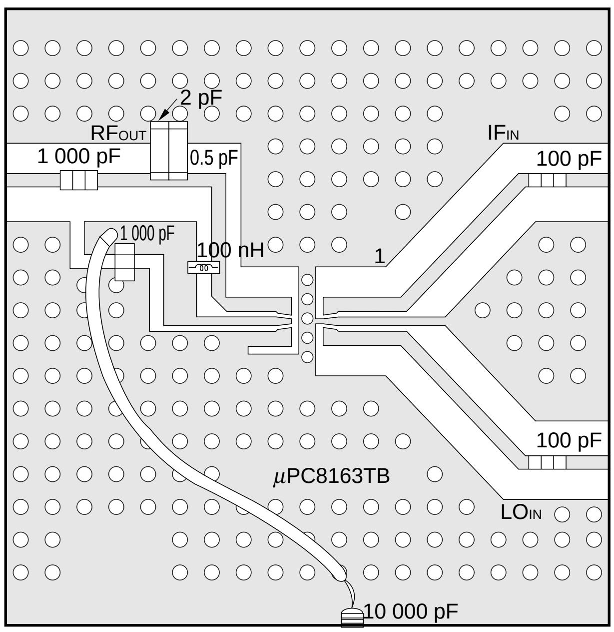
ATTENTION Test circuit or print pattern in this sheet is for testing IC characteristics.

In the case of actual system application, external circuits including print pattern and matching circuit constant of output port should be designed in accordance with IC's S parameters and environmental components.

TEST CIRCUIT 2 (f_{RFout} = 1.9 GHz)



★ **ILLUSTRATION OF TEST CIRCUIT 2 ASSEMBLED ON EVALUATION BOARD**

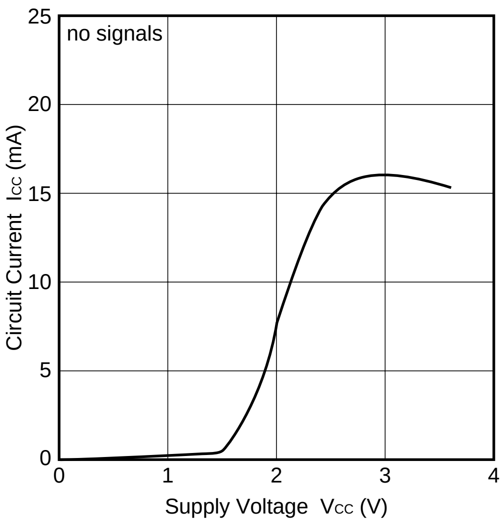


EVALUATION BOARD CHARACTERS

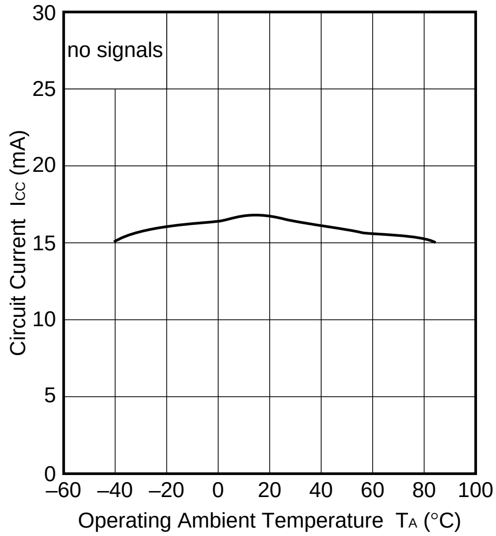
(1) 35 μm thick double-sided copper clad 35 × 42 × 0.4 mm polyimide board
(2) Back side: GND pattern
(3) Solder plated patterns
(4) ○O: Through holes

★ TYPICAL CHARACTERISTICS (T$_A$ = +25°C, unless otherwise specified V$_{CC}$ = V$_{RFout}$)

CIRCUIT CURRENT vs. SUPPLY VOLTAGE

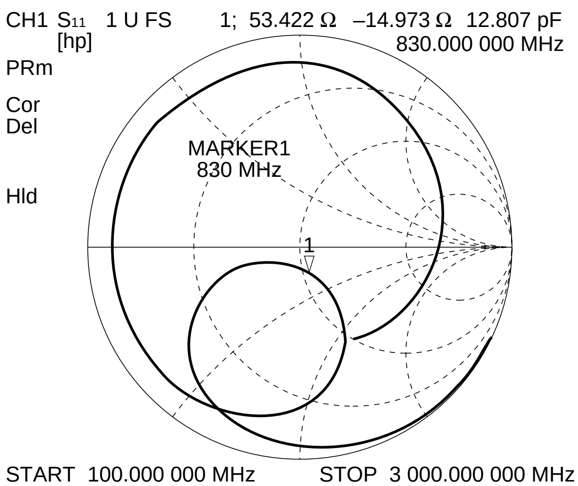


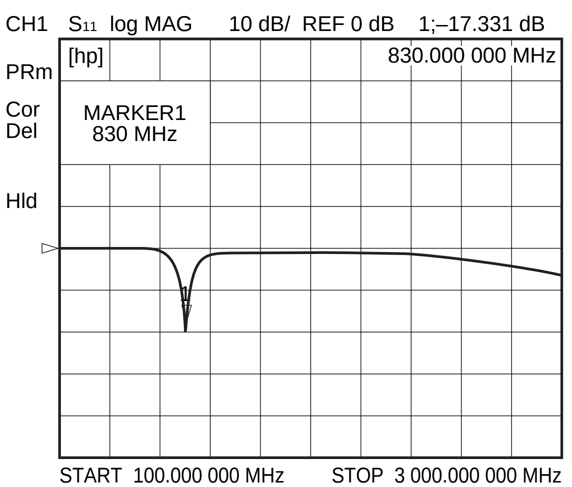
CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE



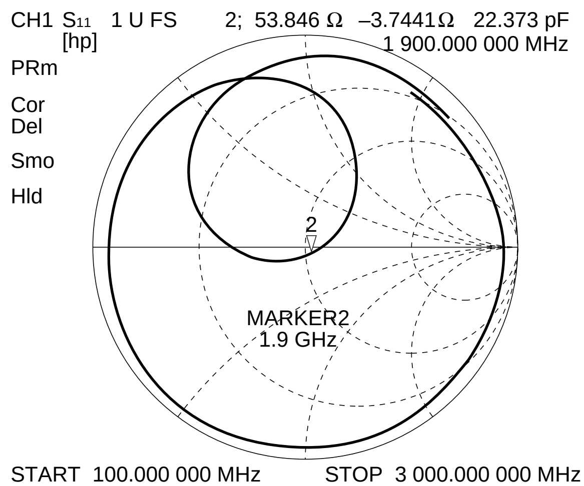
★ S-PARAMETER FOR MATCHED RF OUTPUT (V$_{CC}$ = V$_{RFout}$ = 3.0 V) – with TEST CIRCUITS 1 and 2 – (monitored at RF connector on board)

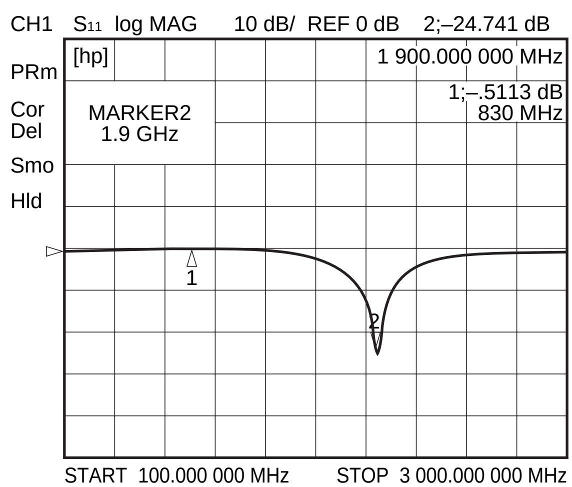
- RF output matched at 830 MHz





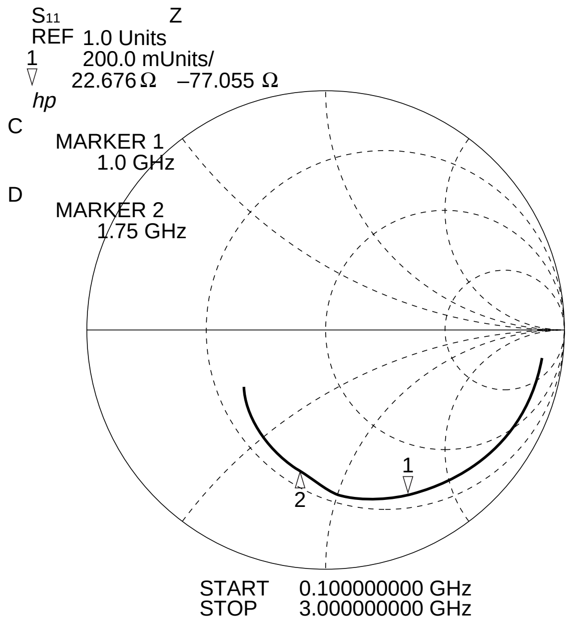
- RF output matched at 1.9 GHz



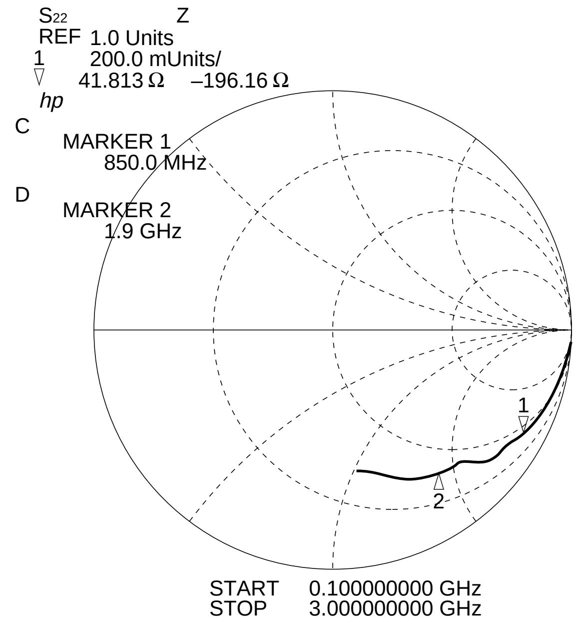


★ **S-PARAMETERS FOR EACH PORT ($V_{CC} = V_{RFout} = 3.0$ V)**

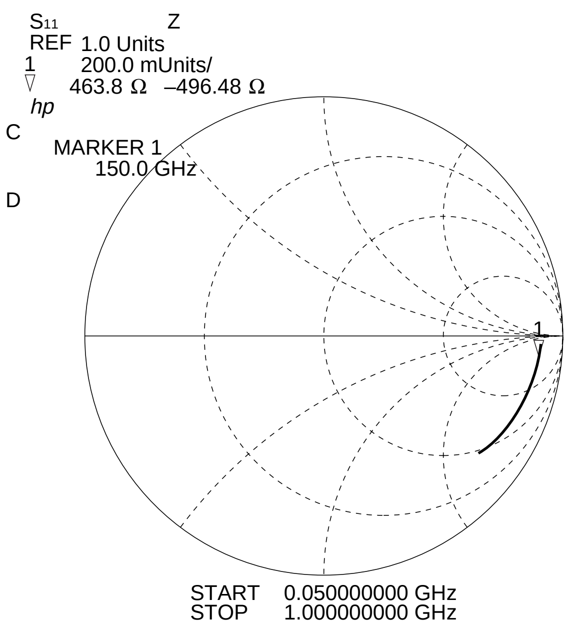
LO port



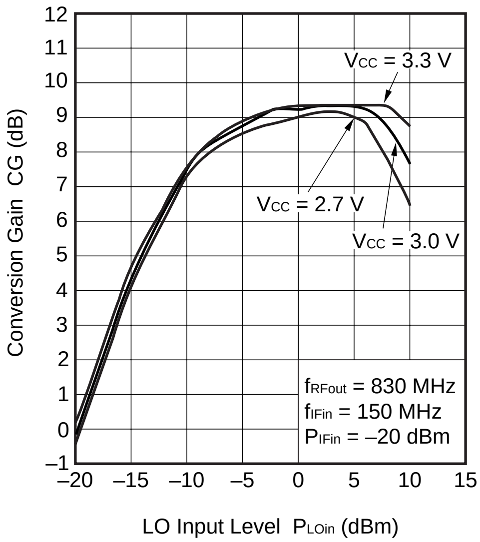
RF port (no matching)



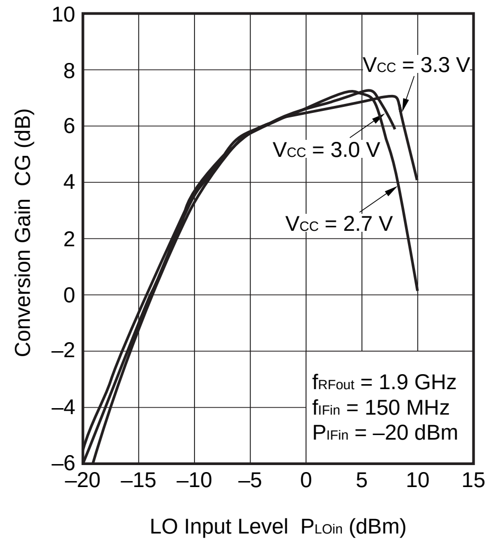
IF port



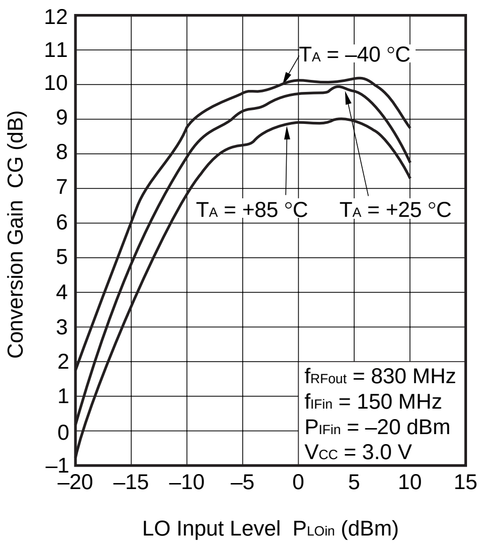
CONVERSION GAIN vs. LO INPUT LEVEL



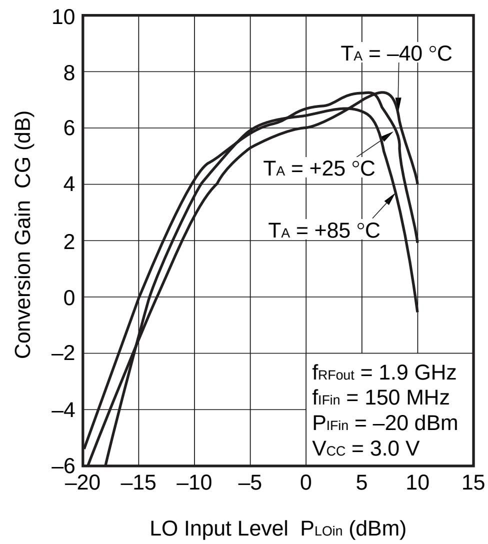
CONVERSION GAIN vs. LO INPUT LEVEL



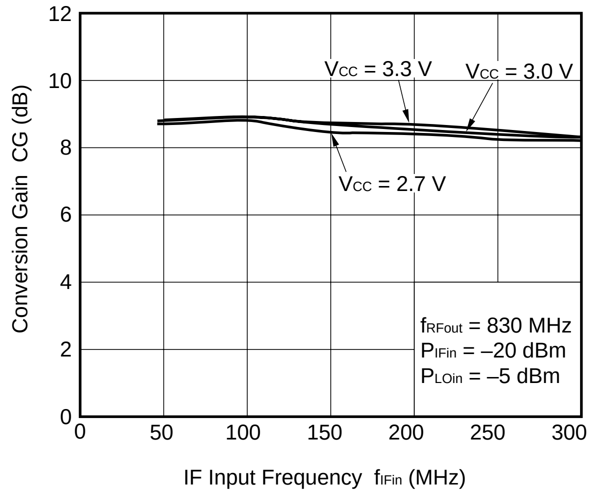
CONVERSION GAIN vs. LO INPUT LEVEL



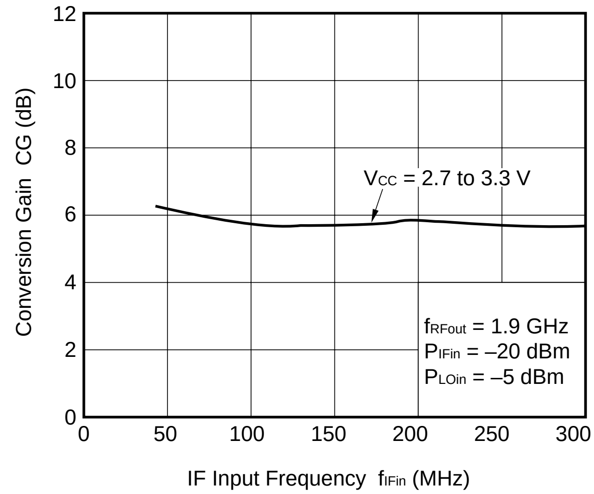
CONVERSION GAIN vs. LO INPUT LEVEL



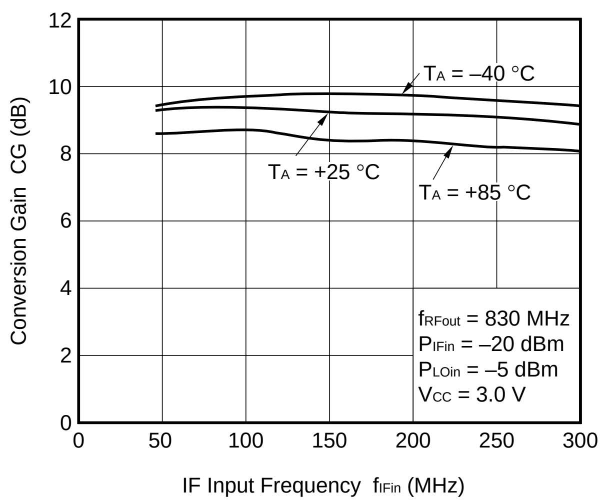
CONVERSION GAIN vs. IF INPUT FREQUENCY



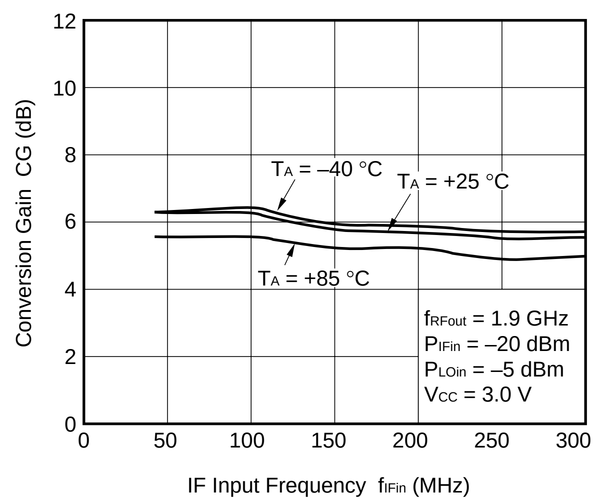
CONVERSION GAIN vs. IF INPUT FREQUENCY



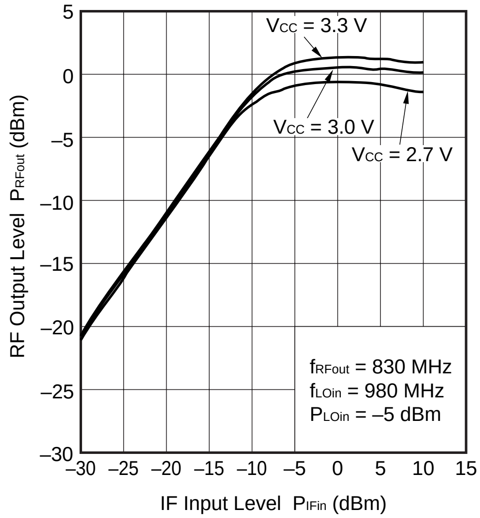
CONVERSION GAIN vs. IF INPUT FREQUENCY



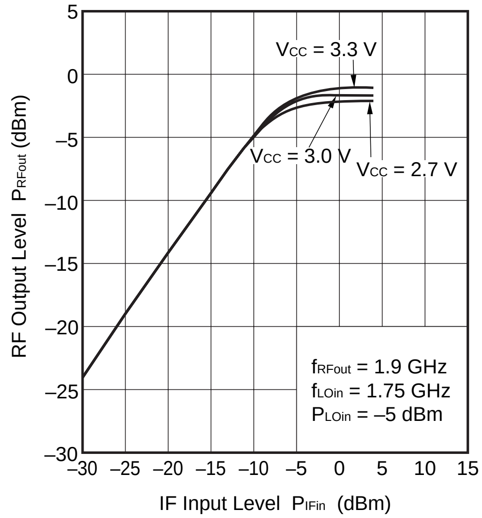
CONVERSION GAIN vs. IF INPUT FREQUENCY



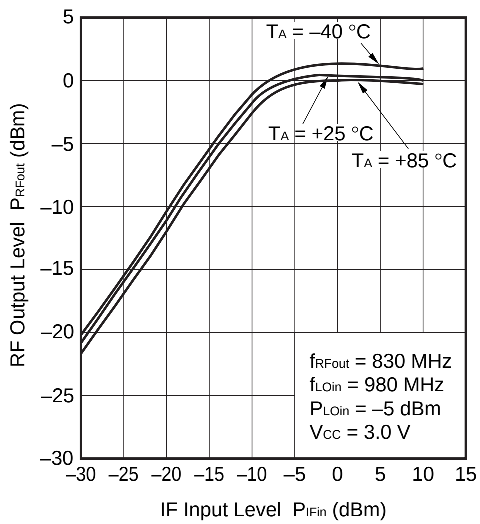
RF OUTPUT LEVEL vs. IF INPUT LEVEL



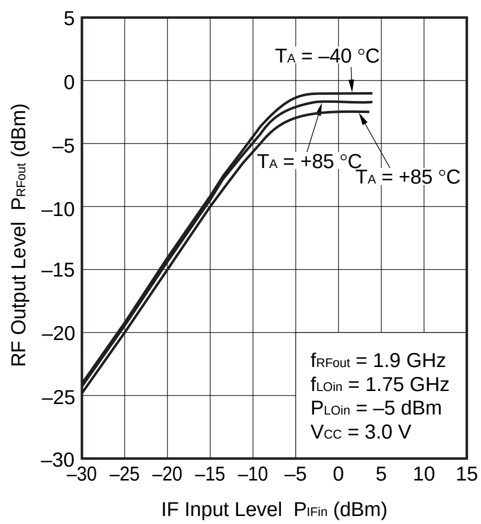
RF OUTPUT LEVEL vs. IF INPUT LEVEL



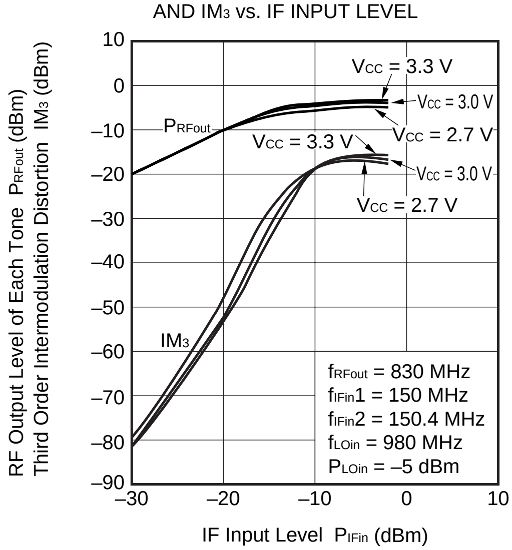
RF OUTPUT LEVEL vs. IF INPUT LEVEL



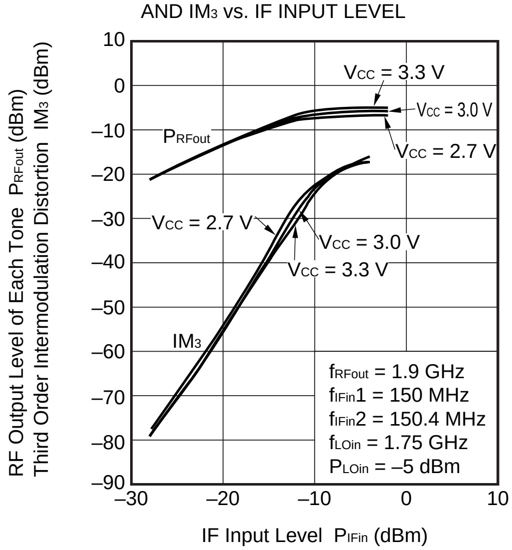
RF OUTPUT LEVEL vs. IF INPUT LEVEL



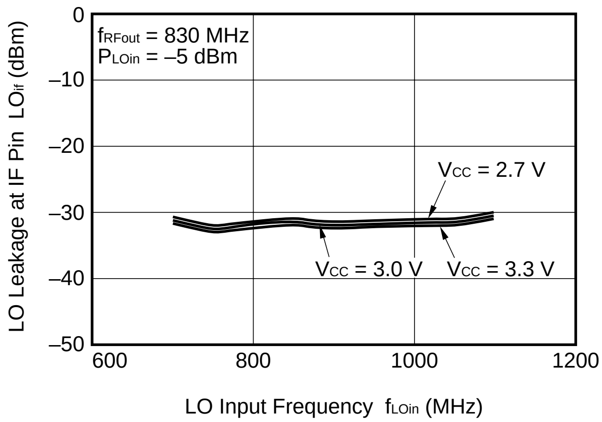
RF OUTPUT LEVEL OF EACH TONE AND IM3 vs. IF INPUT LEVEL



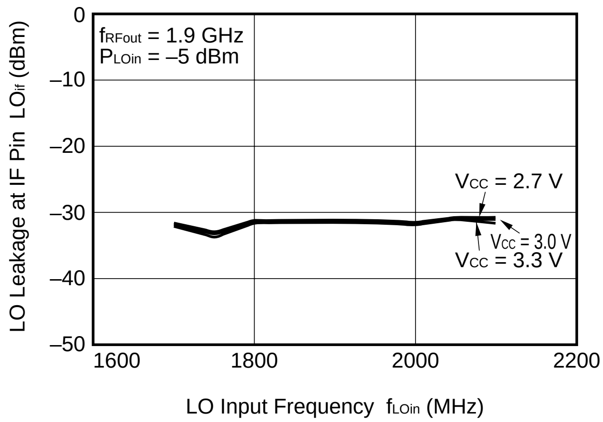
RF OUTPUT LEVEL OF EACH TONE AND IM3 vs. IF INPUT LEVEL



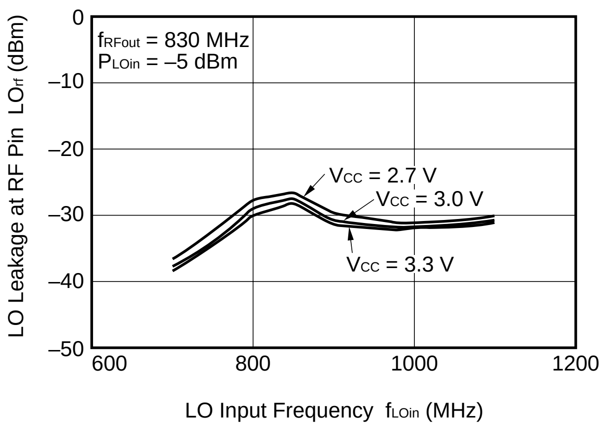
LO LEAKAGE AT IF PIN vs. LO INPUT FREQUENCY



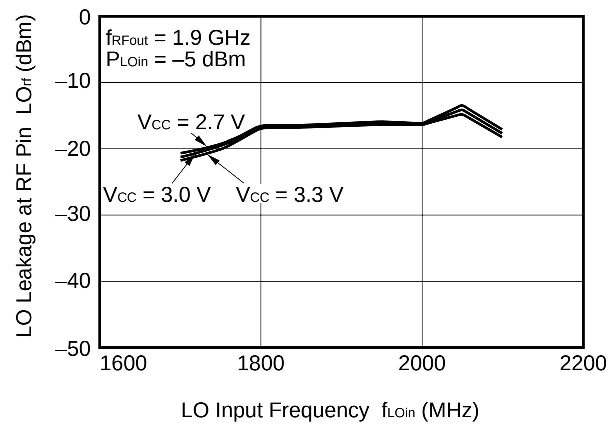
LO LEAKAGE AT IF PIN vs. LO INPUT FREQUENCY



LO LEAKAGE AT RF PIN vs. LO INPUT FREQUENCY

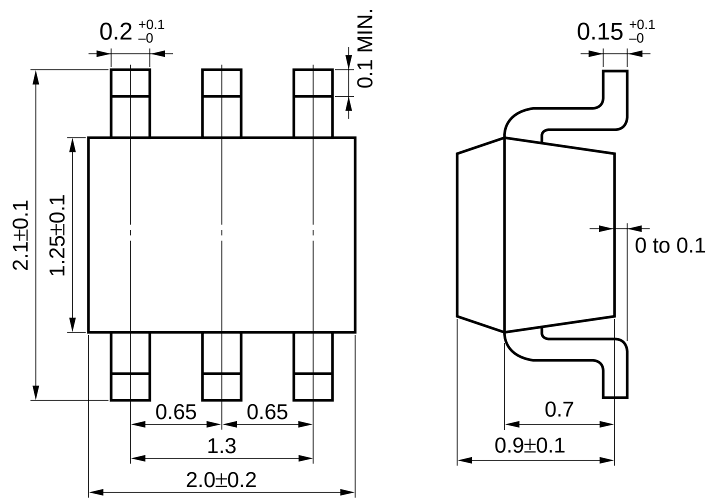


LO LEAKGE AT RF PIN vs. LO INPUT FREQUENCY



PACKAGE DIMENSIONS

6 pin super minimold (Unit: mm)



NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern as wide as possible to keep the minimum ground impedance (to prevent undesired oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor (example: 1 000 pF) to the V_{CC} pin.

RECOMMENDED SOLDERING CONDITIONS

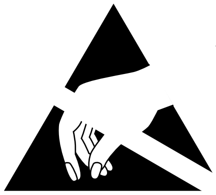
This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235 °C or below Time: 30 seconds or less (at 210 °C) Count: 3, Exposure limit: None[Note]	IR35-00-3
VPS	Package peak temperature: 215 °C or below Time: 40 seconds or less (at 200 °C) Count: 3, Exposure limit: None[Note]	VP15-00-3
Wave Soldering	Soldering bath temperature: 260 °C or below Time: 10 seconds or less Count: 1, Exposure limit: None[Note]	WS60-00-1
Partial Heating	Pin temperature: 300 °C Time: 3 seconds or less (per side of device) Exposure limit: None[Note]	–

Note After opening the dry pack, keep it in a place below 25 °C and 65 % RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).



ATTENTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

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